Listing Of Claims

1. (Original) A method for testing a variety of circuit boards for a family of large electronic systems comprising;

establishing a tester on-site with a third-party manufacturer/assembler/tester, said on-site tester having a connector mechanism for connection to each of said variety of circuit boards,

translating a high-level language description file containing a high level language description of hardware for one of said variety of circuit boards into a low level vector format file,

providing said low level vector format file for said one of said variety of circuit boards to said third-party manufacturer/assembler/tester, wherein said low level vector format file contains a test string for said one of said variety of circuit boards be tested, and

wherein from said low level vector format test strings said third-party manufacturer/assembler/tester can establish a set of test vectors to use in performing a scan test on substantially said each one of said variety of circuit boards in said on-site tester.

2. (Original) The method of claim 1 wherein said low level vector format is SVF format.

3. (Original) The method of claim 2 wherein said low level vector format files include a vector file and an isolation file.

4. (Original) The method of claim 1 wherein said high-level language is Tcl.

5. (Original) The method of claim 1 further comprising applying said set of established test vectors in performing a scan test on one of said each one of said variety of circuit boards.

6. (Original) The method of claim 5 wherein prior to applying said set of established test vectors, applying test vectors derived from net list and BSDL data for static testing.

7. (Original) The method of claim 1 wherein said low level vector format file contains SVF formatted static test data useful for internal ASIC static scan testing.

8. (Original) The method of claim 1 wherein said low level vector format file contains SVF formatted dynamic test data useful for at-speed testing.

9. (Original) The method of claim 1 wherein a unique SVF formatted file is created for each version of said one of said variety of circuit boards.

10. (Original) The method of claim 1 wherein said SVF formatted file is downloaded into said on-site tester directly from an owner.

11. (Original) The method of claim 1 further comprising during an installation step in which a unitary board of one of said variety of circuit boards is fitted into said tester for testing, wherein a symbolic code on a surface of said unitary board is read to determine which test vectors will be used for testing said unitary board.

12. (Original) The method of claim 11 wherein said symbolic code is a bar code and said bar code is unique for each unitary board of each of said variety of boards.

13. (Original) The method of claim 11 wherein said symbolic code provides a unique identifier for tracking said each unitary board.

14. (Original) The method of claim 11 wherein said symbolic code is a bar code and said bar code is unique for each version of said one of said variety of boards, thus providing granularity down to a version level in said determining of which test vectors will be used for testing unitary boards.

15. (Original) The method of claim 1 wherein said translating step comprises restating any proprietary format statements from said high level language into low level statements and using a file of all relevant low level statements for building a vector file containing test vectors, and wherein said vector file is ordered appropriately for use to effectively scan through a TAP interface to said one of said variety of circuit boards into appropriate scan

registers on a unitary board of said one of said variety of circuit boards that is under test.

16. (Original) The method of claim 1 wherein said translating step comprises building an isolation file for later use in comparing to any found errors which are accumulated from a testing step wherein said testing step includes reading output of a test vector result from testing a unitary board, and wherein said comparing produces an indication of error type and physical circuit location where error indicates a problem with the unitary circuit board.

17. (Original) The method of claim 16 further comprising creating a file having a list of any errors and indications of the problem the error indicates.

18. (Original) The method of claim 17 further comprising printing a receipt having human readable information taken from said file having said list of any errors and indications, said receipt for association with said unitary board.

19. (Original) The method of claim 1 further comprising testing said one of said variety of boards by

initializing into a test mode by loading a particular state pattern onto a unitary board after fitting said unitary board into said tester,

allowing to run functional clocks linked to said fitted unitary board for an amount of time sufficient for a test to run with an amount of clock pulses equal to or greater than the number required for the test to be completed,

examining the state of said unitary board to see if it matches expected results.

20. (Original) The method of claim 1 further comprising assembling a computer system with said unitary board.

21. (Original) The computer system assembled in the process of claim 20.

22. (Cancelled)

23. (Currently Amended) The method of claim 24 ~~22~~ further comprising;

producing a receipt of likely faults to be associated physically with said circuit board

being tested.

24. (Currently Amended) ~~A method as set forth in claim 22~~
A method of testing multiple non-identical models of circuit boards of different models using a single test apparatus comprising,

providing software data useful to test said non-identical models of circuit boards to a computer facility associated with said test apparatus

determining which model of said non-identical circuit board is to be tested

electrically connecting a one of said models of said non-identical circuit boards to be tested to the test apparatus,

applying the appropriate test software for said model to said circuit board being tested to said computer facility based on said determining step, and

running said appropriate test software for said model,

wherein, said supplying the software to test each circuit board model, is completed by

a) delivery of said software to a subcontractor for use in said computer associated with said test apparatus in said subcontractor's facilities, and

b) by said subcontractor formatting test vectors in said software into a form suitable for use in said circuit board model.

25. (Currently Amended) The method of claim 24 ~~22~~ wherein said subcontractor develops test vectors from said software to produce said appropriate test software from said provided software.